

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-329813  
(43)Date of publication of application : 15.11.2002

(51)Int.CI. H01L 23/12  
H01L 21/56

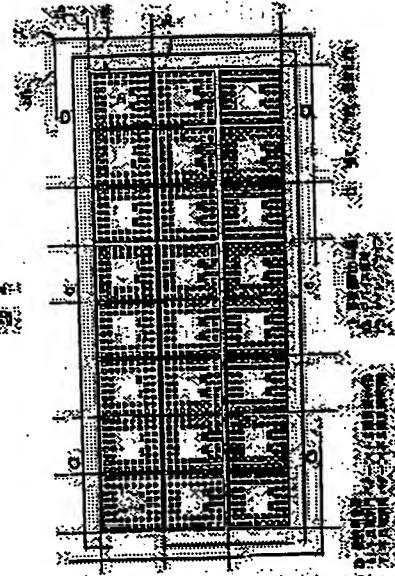
(21)Application number : 2001-131574 (71)Applicant : HITACHI LTD  
(22)Date of filing : 27.04.2001 (72)Inventor : TSUTSUMI YASUKI  
MIWA TAKASHI  
KURODA HIROSHI

## (54) MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICE

### (57)Abstract:

**PROBLEM TO BE SOLVED:** To efficiently and easily select semiconductor devices, and to reduce a manufacturing cost.

**SOLUTION:** In the semiconductor device formed by a MAP system, patterns 6 and 7 for defective identification are formed on the soldered-bump forming surfaces of a printed wiring board. These patterns 6 and 7 for defective identification represent patterns for a display identifying the defective semiconductor device, markings are put on the patterns 6 for defective identification when there is a defectiveness such as a defective wiring in the printed wiring board, and markings are put on the patterns 7 for defective identification when the defectiveness is generated in an assembly process. The markings are put on either of the patterns 6 or 7 for defective identification by flawing by a cutter or the like or the coating of ink or the like. Accordingly, the semiconductor device in the defective printed wiring board or a defective assembly can be removed efficiently in a short time.



### LEGAL STATUS

[Date of request for examination] 18.10.2004

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

BEST AVAILABLE COPY

\* NOTICES \*

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

---

CLAIMS

---

[Claim(s)]

[Claim 1] Have two or more device fields and a defect discernment display is formed in the external electrode forming face of said device field, respectively. The process by which marking was carried out to said defect discernment display of the device field where the defect was detected by inspection of electrical characteristics among said two or more device fields and for which many picking substrates are prepared, The process for which the semiconductor chip carried in said two or more device fields is prepared, The process which carries said semiconductor chip in said device field by which marking is not carried out to said defect discernment display, The process which connects the surface electrode of said semiconductor chip, and the bonding electrode of said device field corresponding to this by the connection member, The process which conducts defect inspection of said device field where the surface electrode of said semiconductor chip and the bonding electrode of said device field corresponding to this were connected by said connection member, The process which carries out marking to the defect discernment display of said device field where the defect was detected, The process which forms the package closure section while covering to a package said two or more device fields which can be set to a picking substrate with mold resin and carrying out the resin seal of said semiconductor chip, A dicing line is met. For said every device field Said process which divides and piece[ of an individual ]-izes a majority of picking substrates and said package closure sections, and forms each closure section, The manufacture approach of the semiconductor device characterized by having the process which detects marking of said defect discernment display and removes said closure section of a defect.

[Claim 2] Have two or more device fields and a defect discernment display is formed in the external electrode forming face of said device field, respectively. The process by which marking was carried out to said defect discernment display of the device field where the defect was detected by inspection of electrical characteristics among said two or more device fields and for which many picking substrates are prepared, The process for which the semiconductor chip carried in said two or more device fields is prepared, The process which carries said semiconductor chip in said device field by which marking is not carried out to said defect discernment display, The process which connects the surface electrode of said semiconductor chip, and the bonding electrode of said device field corresponding to this by the connection member, The process which conducts defect inspection of said device field where the surface electrode of said semiconductor chip and the bonding electrode of said device field corresponding to this were connected by said connection member, The process which carries out marking to the defect discernment display of said device field where the defect was detected, The process which forms the package closure section while covering to a package said two or more device fields which can be set to a picking substrate with mold resin and carrying out the resin seal of said semiconductor chip, The process which conducts defect inspection of said package closure section, and the process which carries out marking to the defect discernment display of said device field where the defect was detected, A dicing line is met. For said every device field Said process which divides and piece[ of an individual ]-izes a majority of picking substrates and said package closure sections, and forms each closure section, The manufacture approach of the semiconductor device characterized by having the process which detects marking of said defect discernment display and removes said closure section of a defect.

[Claim 3] Have two or more device fields and a defect discernment display is formed in the external electrode forming face of said device field, respectively. The process by which marking was carried out to said defect discernment display of the device field where the defect was detected by inspection of electrical characteristics among said two or more device fields and for which many picking substrates are prepared, The process for which the semiconductor chip carried in said two or more device fields is prepared, The process which carries said semiconductor chip in said device field by which marking is not carried out to said defect discernment display, The process which connects the surface electrode of said semiconductor chip, and the bonding electrode of said device field corresponding to this by the connection member, The process which conducts defect inspection of

· said device field where the surface electrode of said semiconductor chip and the bonding electrode of said device field corresponding to this were connected by said connection member, The process which carries out marking to the defect discernment display of said device field where the defect was detected, The process which forms the package closure section while covering to a package said two or more device fields which can be set to a picking substrate with mold resin and carrying out the resin seal of said semiconductor chip, The process which conducts defect inspection of said package closure section, and the process which carries out marking to the defect discernment display of said device field where the defect was detected, The process which forms an external electrode in the external electrode forming face of said device field, and the process which performs defect detection of an external electrode, The process which carries out marking to the defect discernment display of said device field where the defect was detected, A dicing line is met. For said every device field Said process which divides and piece[ of an individual ]-izes a majority of picking substrates and said package closure sections, and forms each closure section, The manufacture approach of the semiconductor device characterized by having the process which detects marking of said defect discernment display and removes said closure section of a defect.

[Claim 4] Have two or more device fields and a defect discernment display is formed in the external electrode forming face of said device field, respectively. The process by which marking was carried out to said defect discernment display of the device field where the defect was detected by inspection of electrical characteristics among said two or more device fields and for which many picking substrates are prepared, The process for which the semiconductor chip carried in said two or more device fields is prepared, The process which carries said semiconductor chip in said device field by which marking is not carried out to said defect discernment display, The process which connects the surface electrode of said semiconductor chip, and the bonding electrode of said device field corresponding to this by the connection member, The process which conducts defect inspection of said device field where the surface electrode of said semiconductor chip and the bonding electrode of said device field corresponding to this were connected by said connection member, The process which carries out marking to the defect discernment display of said device field where the defect was detected, The process which forms the package closure section while covering to a package said two or more device fields which can be set to a picking substrate with mold resin and carrying out the resin seal of said semiconductor chip, The process which conducts defect inspection of said package closure section, and the process which carries out marking to the defect discernment display of said device field where the defect was detected, The process which forms an external electrode in the external electrode forming face of said device field, and the process which performs defect detection of an external electrode, The process which carries out marking to the defect discernment display of said device field where the defect was detected, A dicing line is met. For said every device field Said process which divides and piece[ of an individual ]-izes a majority of picking substrates and said package closure sections, and forms each closure section, The manufacture approach of the semiconductor device characterized by having the process which detects the defect of each closure section of said, the process which carries out marking to the defect discernment display of said device field where the defect was detected, and the process which detects marking of said defect discernment display and removes said closure section of a defect.

[Claim 5] The 6th defect discernment display is formed, respectively. two or more device fields — having — the external electrode forming face of said device field — the 1— The process by which marking was carried out to said 1st defect discernment display of the device field where the defect was detected by inspection of electrical characteristics among said two or more device fields and for which many picking substrates are prepared, The process for which the semiconductor chip carried in said two or more device fields is prepared, The process which carries said semiconductor chip in said device field by which marking is not carried out to said 1st defect discernment display, The process which connects the surface electrode of said semiconductor chip, and the bonding electrode of said device field corresponding to this by the connection member, The process which conducts defect inspection of said device field where the surface electrode of said semiconductor chip and the bonding electrode of said device field corresponding to this were connected by said connection member, When marking is carried out to the 2nd defect discernment display of said device field when the poor bonding of said semiconductor chip is detected, and the faulty connection of said connection member is detected The process which carries out marking to the 3rd defect discernment display of said device field, The process which forms the package closure section while covering to a package said two or more device fields which can be set to a picking substrate with mold resin and carrying out the resin seal of said semiconductor chip, The process which conducts defect inspection of said package closure section, and the process which carries out marking to the 4th defect discernment display of said device field where the defect was detected, The process which forms an external

electrode in the external electrode forming face of said device field, and the process which performs defect detection of said external electrode, The process which carries out marking to the 5th defect discernment display of said device field where the defect was detected, A dicing line is met. For said every device field Said process which divides and piece[ of an individual ]-izes a majority of picking substrates and said package closure sections, and forms each closure section, The process which performs defect detection of each closure section of said, and the process which carries out marking to the 6th defect discernment display of said device field where the defect was detected, said the 1- the manufacture approach of the semiconductor device characterized by having the process which detects marking of the 6th defect discernment display and removes said closure section of a defect.

---

[Translation done.]

**\* NOTICES \***

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

---

**DETAILED DESCRIPTION**

---

**[Detailed Description of the Invention]**

**[0001]**

**[Field of the Invention]** Especially this invention is applied to sorting of the semiconductor device formed by the package mold method (MAP:Mold Array Package) about the manufacturing technology of a semiconductor device, and relates to an effective technique.

**[0002]**

**[Description of the Prior Art]** For example, in the semiconductor device of surface mount form packages, such as CSP (Chip Size Package), the so-called package mold method is learned as a technique of improving productive efficiency and attaining low cost-ization.

**[0003]** According to the place which this invention person examined, a package mold method is the approach of two or more device fields being divided, carrying out the resin seal of two or more device fields which were formed by standing in a row and where many semiconductor chips were carried in each using the printed-circuit board of picking by mold in the state of a wrap at a package, and forming the package closure section.

**[0004]** And external terminals, such as a solder bump, are formed after a resin seal, dicing is performed, much picking printed-circuit boards and package closure sections are divided per device field (formation of the piece of an individual), and each package is formed.

**[0005]** Moreover, when the device field of a printed-circuit board in which a semiconductor chip is carried has poor wiring, the mark of defect discernment which prevents that a semiconductor chip is carried in the device field is prepared in the defect part. As a mark of this defect discernment, it is the marking-off of marking in the seal for defect discernment, ink, etc., or a defect part front face etc., for example.

**[0006]** Then, screening from which the piece[ of an individual ]-ized semiconductor device removes the product of a potential defect etc. in a sorting process is performed, and the judgment of an excellent article and a defective is performed.

**[0007]** In addition, as an example to which this kind of semiconductor device is stated in detail, there is JP,12-12745,A and the semiconductor device assembled using a package mold method is indicated by this reference.

**[0008]**

**[Problem(s) to be Solved by the Invention]** However, it was found out by this invention person in the manufacturing technology in the semiconductor device of the above MAP methods that there are the following troubles.

**[0009]** That is, since the mark of defect discernment cannot distinguish from an appearance in the semiconductor device piece[ of an individual ]-ized after performing a resin seal collectively, management of a defective is

difficult.

[0010] Therefore, in a sorting process, while having to conduct screening inspection of all semiconductor devices, the time amount concerning screening of this sorting process becoming long and the manufacture effectiveness of a semiconductor device becoming low, judgment of at which process the semiconductor device distinguished from the defect was generated is difficult, and there is a problem that failure analysis is difficult.

[0011] The purpose of this invention sorts out a semiconductor device efficiently and easily, and is to offer the manufacture approach of the semiconductor device which can make a manufacturing cost small.

[0012] The other purposes and the new description will become clear from description and the accompanying drawing of this specification along [ said ] this invention.

[0013]

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.

[0014] Namely, the manufacture approach of the semiconductor device of this invention Have two or more device fields and a defect discernment display is formed in the external electrode forming face of this device field, respectively. The process by which marking was carried out to the defect discernment display of the device field where the defect was detected by inspection of electrical characteristics among two or more device fields and for which many picking substrates are prepared, The process for which the semiconductor chip carried in two or more device fields is prepared, and the process which carries said semiconductor chip in the device field by which marking is not carried out to a defect discernment display, The process which connects the surface electrode of a semiconductor chip, and the bonding electrode of the device field corresponding to this by the connection member, The process which conducts defect inspection of the device field where the surface electrode of a semiconductor chip and the bonding electrode of the device field corresponding to this were connected by the connection member, The process which carries out marking to the defect discernment display of the device field where the defect was detected, The process which forms the package closure section while covering to a package two or more device fields which can be set to a picking substrate with mold resin and carrying out the resin seal of the semiconductor chip, Much picking substrates and package closure sections are divided and piece[ of an individual ]-ized for every device field along a dicing line, and it has the process which forms each closure section, and the process which detects the defect identification marking formed in the defect discernment display, and removes a defect's closure section.

[0015] Moreover, the manufacture approach of the semiconductor device of this invention has two or more device fields. A defect discernment display is formed in the external electrode forming face of this device field, respectively. The process by which marking was carried out to the defect discernment display of the device field where the defect was detected by inspection of electrical characteristics among two or more device fields and for which many picking substrates are prepared, The process for which the semiconductor chip carried in two or more device fields is prepared, and the process which carries a semiconductor chip in the device field by which marking is not carried out to a defect discernment display, The process which connects the surface electrode of a semiconductor chip, and the bonding electrode of the device field corresponding to this by the connection member, The process which conducts defect inspection of the device field where the surface electrode of a semiconductor chip and the bonding electrode of the device field corresponding to this were connected by the connection member, The process which carries out marking to the defect discernment display of said device field where the defect was detected, The process which forms the package closure section while covering to a package two or more device fields which can be set to a picking substrate with mold resin and carrying out the resin seal of the semiconductor chip, The process which conducts defect inspection of the package closure section, and the process which carries out marking to the defect discernment display of said device field where the defect was detected, Much picking substrates and package closure sections are divided and piece[ of an individual ]-ized for every device field along a dicing line, and it has the process which forms each closure section, and the process which detects the defect identification marking formed in the defect discernment display, and removes said closure section of a defect.

[0016] Furthermore, the manufacture approach of the semiconductor device of this invention has two or more device fields. A defect discernment display is formed in the external electrode forming face of this device field, respectively. The process by which marking was carried out to the defect discernment display of the device field where the defect was detected by inspection of electrical characteristics among two or more device fields and for which many picking substrates are prepared, The process for which the semiconductor chip carried in two or more device fields is prepared, and the process which carries a semiconductor chip in the device field by which

marking is not carried out to a defect discernment display, The process which connects the surface electrode of a semiconductor chip, and the bonding electrode of the device field corresponding to this by the connection member, The process which conducts defect inspection of the device field where the surface electrode of a semiconductor chip and the bonding electrode of the device field corresponding to this were connected by the connection member, The process which carries out marking to the defect discernment display of the device field where the defect was detected, The process which forms the package closure section while covering to a package two or more device fields which can be set to a picking substrate with mold resin and carrying out the resin seal of the semiconductor chip, The process which conducts defect inspection of the package closure section, and the process which carries out marking to the defect discernment display of said device field where the defect was detected, The process which forms an external electrode in the external electrode forming face of a device field, and the process which performs defect detection of an external electrode, The process which carries out marking to the defect discernment display of the device field where the defect was detected, Much picking substrates and package closure sections are divided and piece[ of an individual ]-ized for every device field along a dicing line, and it has the process which forms each closure section, and the process which detects the defect identification marking formed in the defect discernment display, and removes said closure section of a defect.

[0017] Moreover, the manufacture approach of the semiconductor device of this invention has two or more device fields. A defect discernment display is formed in the external electrode forming face of this device field, respectively. The process by which marking was carried out to the defect discernment display of the device field where the defect was detected by inspection of electrical characteristics among two or more device fields and for which many picking substrates are prepared, The process for which the semiconductor chip carried in two or more device fields is prepared, and the process which carries a semiconductor chip in the device field by which marking is not carried out to a defect discernment display, The process which connects the surface electrode of a semiconductor chip, and the bonding electrode of the device field corresponding to this by the connection member, The process which conducts defect inspection of the device field where the surface electrode of a semiconductor chip and the bonding electrode of the device field corresponding to this were connected by the connection member, The process which carries out marking to the defect discernment display of the device field where the defect was detected, The process which forms the package closure section while covering to a package two or more device fields which can be set to a picking substrate with mold resin and carrying out the resin seal of the semiconductor chip, The process which conducts defect inspection of this package closure section, and the process which carries out marking to the defect discernment display of the device field where the defect was detected, The process which forms an external electrode in the external electrode forming face of a device field, and the process which performs defect detection of an external electrode, The process which carries out marking to the defect discernment display of the device field where the defect was detected, The process which divides and piece[ of an individual ]-izes much picking substrates and package closure sections for every device field along a dicing line, and forms each closure section, It has the process which detects the defect of each closure section, the process which carries out marking to the defect discernment display of the device field where the defect was detected, and the process which detects the defect identification marking formed in the defect discernment display, and removes a defect's closure section.

[0018] Furthermore, the manufacture approach of the semiconductor device of this invention has two or more device fields. The 6th defect discernment display is formed, respectively, the external electrode forming face of this device field — the 1- The process by which marking was carried out to the 1st defect discernment display of the device field where the defect was detected by inspection of electrical characteristics among two or more device fields and for which many picking substrates are prepared, The process for which the semiconductor chip carried in two or more device fields is prepared, and the process which carries a semiconductor chip in the device field by which marking is not carried out to the 1st defect discernment display, The process which connects the surface electrode of a semiconductor chip, and the bonding electrode of the device field corresponding to this by the connection member, The process which conducts defect inspection of the device field where the surface electrode of a semiconductor chip and the bonding electrode of the device field corresponding to this were connected by the connection member, When marking is carried out to the 2nd defect discernment display of a device field when the poor bonding of a semiconductor chip is detected, and the faulty connection of a connection member is detected The process which carries out marking to the 3rd defect discernment display of a device field, and the process which forms the package closure section while covering to a package two or more device fields which can be set to a picking substrate with mold resin and carrying out the resin seal of the

semiconductor chip, The process which conducts defect inspection of the package closure section, and the process which carries out marking to the 4th defect discernment display of the device field where the defect was detected, The process which forms an external electrode in the external electrode forming face of a device field, and the process which performs defect detection of an external electrode, The process which carries out marking to the 5th defect discernment display of the device field where the defect was detected, The process which divides and piece[ of an individual ]-izes much picking substrates and package closure sections for every device field along a dicing line, and forms each closure section, the process which performs defect detection of each closure section, the process which carries out marking to the 6th defect discernment display of the device field where the defect was detected, and the 1- the defect identification marking formed in the 6th defect discernment display is detected, and it has the process which removes a defect's closure section.

[0019]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail based on a drawing.

[0020] The explanatory view and drawing 12 which showed the example of a display of the pattern for defect discernment with which the explanatory view of a production process [ in / drawing 3 / an appearance perspective view / in / in the sectional view of the semiconductor device according / drawing 1 / to the gestalt of 1 operation of this invention and drawing 2 / the semiconductor device of drawing 1 / and / in the bottom view of the semiconductor device of drawing 1 , drawing 4 - drawing 10 / the semiconductor device of drawing 1 ] and drawing 11 were formed in a defect's semiconductor device are the flow chart of the production process in the semiconductor device of drawing 1 .

[0021] In the gestalt of this operation, a semiconductor device 1 consists of BGA (Ball Grid Array) which is one of the surface mount form packages, and is formed by the MAP method.

[0022] As this semiconductor device 1 is shown in drawing 1 and drawing 2 , the printed-circuit board 2 which consists of a glass epoxy resin etc. is formed. Except a printed circuit board is sufficient as a printed-circuit board 2, for example, you may make it constitute it here using tape substrates, such as polyimide.

[0023] The semiconductor chip 4 is carried in the principal plane (semiconductor chip loading side) center section of the printed-circuit board 2 through the binders 3, such as insulating resin. In the principal plane of a printed-circuit board 2, bonding electrode 2a and a circuit pattern are formed near [ where a semiconductor chip 4 counters ] the periphery of two sides.

[0024] Electrode 2b for connection ( drawing 4 ) arranged in the shape of an array and a circuit pattern are formed in the rear face of a printed-circuit board 2. Bonding electrode 2a and electrode 2b for connection are electrically connected by the circuit pattern formed in both sides of a printed-circuit board, the through hole, etc.

[0025] Moreover, two or more solder bumps (external electrode) 5 who consist of globular form solder are formed in electrode 2b for connection of printed-circuit board 2 rear face, respectively. These solder bump 5 is arranged in the shape of [ which is constituted by a multi-line / two or more trains (here two line x2 train) on the rear face of a printed-circuit board 2 ] an array, as shown in drawing 3 .

[0026] Furthermore, near the core of printed-circuit board 2 rear face, the rectangle-like patterns 6 and 7 for defect discernment (defect discernment display) are formed. The patterns 6 and 7 for these defect discernment consist of a configuration that gilding was given to the circuit pattern formed in the printed-circuit board 2.

[0027] The patterns 6 and 7 for these defect discernment are patterns for a display which identify the defect of a semiconductor device 1. The pattern 6 for defect discernment located in the left-hand side of drawing 3 is a viewing area by which marking is carried out in the case of the printed-circuit board 2 with poor wiring, and when the pattern 7 for defect discernment located in right-hand side is set like an assembler and a defect occurs, it is a viewing area by which marking is carried out.

[0028] Marking of defect discernment is performed to the patterns 6 and 7 for these defect discernment by applying ink etc. to either of these patterns 6 and 7 for defect discernment. Moreover, marking of defect discernment may give a crack to the patterns 6 and 7 for defect discernment by a cutter etc. in addition to spreading of ink, or you may make it remove this pattern 6 for defect discernment, and 7 itself.

[0029] As shown in drawing 1 and drawing 2 , two or more electrode (surface electrode) 4a is formed in the principal plane of a semiconductor chip 4 near the periphery section of this semiconductor chip 4. As for these electrode 4a, predetermined bonding electrode 2a is connected through the bonding wire (connection member) 8, respectively.

[0030] And the closure of the bonding electrode 2a circumference of these semiconductor chips 4 and a printed-circuit board 2 and the bonding wire 8 is carried out with closure resin 9, and the package (closure section) is

formed.

[0031] Furthermore, in case a semiconductor device 1 is mounted in the print mounting substrate which mounts electronic parts etc., the polymerization of the solder bump 5 is carried out to electrodes, such as a land formed in this print mounting substrate 2, she is carried in them, and it connects with them electrically by performing a reflow.

[0032] Next, the explanatory view of the pattern [ in / production process / of the semiconductor device 1 in the gestalt of this operation / the explanatory view of the production process of drawing 1 – drawing 3 and drawing 4 – drawing 10 , and the semiconductor device of the defect of drawing 11 ] for defect discernment and drawing It explains using a flow chart.

[0033] First, the semiconductor chip 4 carried in the picking substrate 10 and this many picking substrate 10 is prepared (step S101). [ many ] As a large number are shown in the picking substrate 10 at drawing 4 , this device field 10a by which matrix arrangement of the plurality was carried out, and dicing line 10b which separates these device field 10a are formed, and the package mold by which resin mold is carried out to a package in the state of a wrap in these two or more device field 10a is given.

[0034] Dicing line 10b is the device field 10a part which becomes a pair, and a field which separates many picking substrates 10 and device field 10a parts. Bonding electrode 2a mentioned above, a circuit pattern, a through hole, electrode 2b for connection, the patterns 6 and 7 for defect discernment, etc. are fabricated by device field 10a, respectively, and after carrying out dicing and being piece[ of an individual ]-ized, it becomes the printed-circuit board 2 ( drawing 1 ) mentioned above.

[0035] Moreover, the mark for defect discernment of the seal which prevents that a semiconductor chip 4 is carried is beforehand formed in the prepared chip loading side of device field 10a of the defect whom poor wiring generated [ in / in large numbers / the picking substrate 10 ], and marking in ink etc. is beforehand performed to the pattern 6 for defect discernment in the opposite side (forming face of electrode 2b for connection).

[0036] And a binder 3 is applied to the semiconductor chip loading side of all device field 10a except device field 10a by which marking was performed to the pattern 6 for defect discernment; respectively, as shown in drawing 5 , a semiconductor chip 4 is carried and adhesion immobilization is carried out (step S102).

[0037] Then, as shown in drawing 6 , electrode 4a of a semiconductor chip 4 and bonding electrode 2a formed in the picking substrate 10 are joined by the bonding wire 8, respectively, and it connects electrically (step S103). [ much ]

[0038] Termination of wirebonding conducts visual inspection which detects a poor assembly, such as a faulty connection of a bonding wire 8, and an open circuit or a location gap of a semiconductor chip 4, (step S104).

[0039] When a defect is discovered in this visual inspection, as shown in (step S105) and drawing 7 , ink etc. is applied to the pattern 7 for defect discernment currently formed in the solder bump forming face of device field 10a, and marking for defect discernment is performed (step S106).

[0040] And after visual inspection is completed, as shown in drawing 8 , package mold is performed using the mold metal mold for transfer molds (step S107), a semiconductor chip 4 and a bonding wire 8 are closed with closure resin 9, mold resin is stiffened, and the package mold section (package closure section) 11 is formed. In addition, as mold resin, the thermosetting resin of an epoxy system etc. is used, for example.

[0041] After the package mold section 11 is formed, visual inspection which inspects poor mold is conducted (step S108). When a defect is discovered in this visual inspection, ink etc. is applied to the pattern 7 for defect discernment currently formed in device field 10a of the corresponding defect like processing of (step S109) and step S106, and marking of defect discernment is performed (step S110).

[0042] Then, as shown in drawing 9 , the solder bump 5 is formed in electrode 2b for connection ( drawing 4 ) currently formed in the rear face of the picking substrate 10, respectively (step S111). [ much ]

[0043] The solder bump 5 turns caudad the semiconductor chip 4 loading side of the many picking substrate 10, arranges the fixture for ball loading which carried out vacuum adsorption maintenance of two or more solder bumps 5 to the upper part, and carries and forms a large number in the electrode for connection on each device field 10a from the upper part of the picking substrate 10.

[0044] Visual inspection of whether there is any defect in this solder bump's 5 formation is carried out after these solder bump's 5 formation (step S112). When a defect is discovered by this visual inspection, ink etc. is applied to the pattern 7 for defect discernment currently formed in device field 10a of the corresponding defect like processing of (step S113) and steps S106 and S110, and marking of defect discernment is performed (step S114).

[0045] And along with dicing line 10b of the picking substrate 10, a majority of each device field 10a is piece[ of an individual ]-ized. In this case, as shown in drawing 10 , this package mold section 11 is divided and piece[ of an

individual]-ized by the dicing using the blade B which is a cutting cutting edge for dicing (step S115), and each package is formed.

[0046] Then, visual inspection of the piece[ of an individual]-ized package is conducted (step S116), when a defect is discovered by this visual inspection, ink etc. is applied to the pattern 7 for defect discernment currently formed in device field 10a of the corresponding defect like processing of (step S117) and steps S106, S110, and S114, and marking of defect discernment is performed (step S118).

[0047] After being piece[ of an individual]-ized, a semiconductor device 1 is sorted out by an excellent article and the defective (step S119), and a semiconductor device 1 completes it (step S120).

[0048] Here, since marking in ink is performed to either of the patterns 6 and 7 for defect discernment formed in the printed-circuit board 2 as shown in a defect's semiconductor device 1 at drawing 11, in the case of sorting, this semiconductor device 1 is sorted out by checking one marking of the patterns 6 and 7 for defect discernment formed in the semiconductor device 1.

[0049] Thereby, according to the gestalt of this operation, only the semiconductor device which became the defect of the picking substrate 10 and a poor assembly can be removed efficiently in a short time, and the manufacturing cost of a semiconductor device 1 can be made small.

[0050] Moreover, since many defects by the picking substrate 10 and defects by an assembly process etc. can be distinguished easily, failure analysis of the semiconductor device which became a defect can be made easy.

[0051] Moreover, although considered as the configuration which formed two patterns 6 and 7 for defect discernment in which a large number are assembled with the defect of the picking substrate 10, and the defect of a process is shown in the electrode 2b forming face side for connection of a printed-circuit board 2 with the gestalt of this operation, six patterns 12-17 for defect discernment are formed in semiconductor device 1a, and you may enable it to distinguish a defect process in a detail more, as shown in drawing 13 and drawing 14.

[0052] The pattern 12 for defect discernment (1st defect discernment display) is a pattern by which marking is carried out in the case of a poor substrate, such as poor wiring. Marking of the pattern 13 for defect discernment (2nd defect discernment display) is carried out in the case of the defect at the time of chip bonding, such as a chip location gap, and marking of the pattern 14 for defect discernment (3rd defect discernment display) is carried out in the case of the defect of wirebonding, such as a faulty connection of a bonding wire.

[0053] Furthermore, the pattern 15 for defect discernment (4th defect discernment display) is a pattern by which marking is carried out in the case of poor formation of the package mold section. Marking of the pattern 16 for defect discernment (5th defect discernment display) is carried out in the case of the solder bump's 5 poor formation.

[0054] The pattern 17 for defect discernment (6th defect discernment display) is a pattern by which marking is carried out, when the poor package formation at the time of dicing occurs. And marking of the patterns 12-17 for these defect discernment is carried out by giving a crack by a cutter etc. or applying ink etc.

[0055] Since the defect like an assembler can be displayed in more detail, while being able to remove a defect's semiconductor device efficiently by that cause in a short time, failure analysis can be performed more easily.

[0056] As mentioned above, although invention made by this invention person was concretely explained based on the gestalt of implementation of invention, it cannot be overemphasized that it can change variously in the range which this invention is not limited to the gestalt of said operation, and does not deviate from the summary.

[0057] For example, although considered as the configuration which prepared the pattern for defect discernment near the center section by the side of the electrode forming face for connection in a semiconductor device with the gestalt of said operation, as the patterns 6 and 7 for these defect discernment formed in a semiconductor device 1 are shown in drawing 15, if this electrode 2b for connection is not contacted, a location, a configuration, etc. which are formed do not ask near the periphery section of a printed-circuit board 2 etc.

[0058]

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated by this application is explained briefly.

[0059] (1) Since only many semiconductor devices of the defect of a picking substrate and a poor assembly can be removed efficiently in a short time, the manufacturing cost of a semiconductor device can be made small.

[0060] (2) Since a large number can be assembled with the defect of a picking substrate and the defect in a process can be distinguished easily, failure analysis of the semiconductor device which became a defect can be performed easily and efficiently.

\* NOTICES \*

JP0 and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

---

## DESCRIPTION OF DRAWINGS

---

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view of the semiconductor device by the gestalt of 1 operation of this invention.

[Drawing 2] It is an appearance perspective view in the semiconductor device of drawing 1.

[Drawing 3] It is the bottom view of the semiconductor device of drawing 1.

[Drawing 4] It is the explanatory view of the production process in the semiconductor device of drawing 1.

[Drawing 5] It is the explanatory view of the production process of the semiconductor device following drawing 4.

[Drawing 6] It is the explanatory view of the production process of the semiconductor device following drawing 5.

[Drawing 7] It is the explanatory view of the production process of the semiconductor device following drawing 6.

[Drawing 8] It is the explanatory view of the production process of the semiconductor device following drawing 7.

[Drawing 9] It is the explanatory view of the production process of the semiconductor device following drawing 8.

[Drawing 10] It is the explanatory view of the production process of the semiconductor device following drawing 9.

[Drawing 11] It is the explanatory view having shown the example of a display of the pattern for defect discernment formed in a defect's semiconductor device.

[Drawing 12] It is the flow chart of the production process in the semiconductor device of drawing 1.

[Drawing 13] It is the bottom view of a semiconductor device in which the pattern for defect discernment by the gestalt of other operations of this invention was prepared.

[Drawing 14] It is the expansion explanatory view of the pattern for defect discernment in the semiconductor device of drawing 13.

[Drawing 15] It is the bottom view of a semiconductor device in which the pattern for defect discernment by the gestalt of other operations of this invention was prepared.

[Description of Notations]

1 Semiconductor Device

1a Semiconductor device

2 Printed-circuit Board

2a Bonding electrode

2b The electrode for connection

3 Binder

4 Semiconductor Chip

4a Electrode (surface electrode)

5 Solder Bump (External Electrode)

6 7 Pattern for defect discernment (defect discernment display)

8 Bonding Wire 9 (Connection Member) Closure Resin

10 It is Picking Substrate in Large Numbers.

10a Device field

10b Dicing line

11 Package Mold Section (Package Closure Section)

12 Pattern for Defect Discernment (1st Defect Discernment Display)

13 Pattern for Defect Discernment (2nd Defect Discernment Display)

14 Pattern for Defect Discernment (3rd Defect Discernment Display)

15 Pattern for Defect Discernment (4th Defect Discernment Display)

16 Pattern for Defect Discernment (5th Defect Discernment Display)

17 Pattern for Defect Discernment (6th Defect Discernment Display)

---

[Translation done.]

(19)日本国特許庁 (JP)

(12) 公開特許公報 (A)

(11)特許出願公開番号  
特開2002-329813  
(P2002-329813A)

(43)公開日 平成14年11月15日 (2002.11.15)

(51)Int.Cl.  
H 01 L 23/12  
21/56

識別記号  
501

F I  
H 01 L 23/12  
21/56

テマコード(参考)  
501 W 5 F 0 6 1  
R

審査請求 未請求 請求項の数 5 OL (全 12 頁)

(21)出願番号 特願2001-131574(P2001-131574)

(22)出願日 平成13年4月27日 (2001.4.27)

(71)出願人 000005108

株式会社日立製作所  
東京都千代田区神田駿河台四丁目6番地

(72)発明者 堤 安己

東京都小平市上水本町五丁目20番1号 株  
式会社日立製作所半導体グループ内

(72)発明者 三輪 孝志

東京都小平市上水本町五丁目20番1号 株  
式会社日立製作所半導体グループ内

(74)代理人 100080001

弁理士 筒井 大和

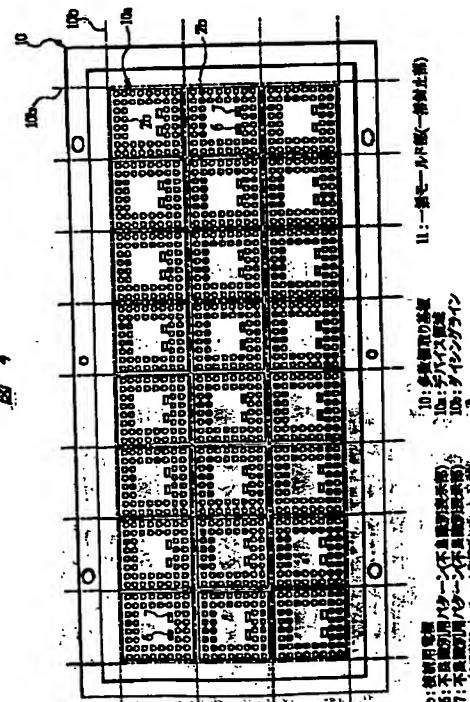
最終頁に続く

(54)【発明の名称】 半導体装置の製造方法

(57)【要約】

【課題】 半導体装置の選別を効率よく、かつ容易に行  
い、製造コストを小さくする。

【解決手段】 MAP方式によって形成される半導体装  
置において、プリント配線基板のはんだバンプ形成面に  
は、不良識別用パターン6, 7が形成されている。これ  
ら不良識別用パターン6, 7は、半導体装置の不良を識  
別する表示用のパターンであり、プリント配線基板に配  
線不良などの不良がある場合には、不良識別用パターン  
6にマーキングが施され、組み立て工程において不良が  
発生した場合には、不良識別用パターン7にマーキング  
が施される。マーキングは、不良識別用パターン6, 7  
のいずれかに、カッターなどによってキズをつけるか、  
あるいはインキなどを塗布する。これにより、プリント  
配線基板の不良、または組み立て不良の半導体装置を短  
時間で効率よく取り除くことができる。





(3)

3

する工程と、

前記不良識別表示部にマーキングされていない前記デバイス領域に前記半導体チップを搭載する工程と、

前記半導体チップの表面電極とこれに対応する前記デバイス領域のボンディング電極とを接続部材によって接続する工程と、

前記半導体チップの表面電極とこれに対応する前記デバイス領域のボンディング電極とが前記接続部材によって接続された前記デバイス領域の不良検査を行う工程と、不良が検出された前記デバイス領域の不良識別表示部にマーキングする工程と、

前記多数個取り基板における複数のデバイス領域をモールド樹脂によって一括に覆い、前記半導体チップを樹脂封止するとともに一括封止部を形成する工程と、

前記一括封止部の不良検査を行う工程と、

不良が検出された前記デバイス領域の不良識別表示部にマーキングする工程と、

前記デバイス領域の外部電極形成面に外部電極を形成する工程と、

外部電極の不良検出を行う工程と、

不良が検出された前記デバイス領域の不良識別表示部にマーキングする工程と、

ダイシングラインに沿って前記デバイス領域毎に前記多数個取り基板および前記一括封止部を分割して個片化し、個々の封止部を形成する工程と、

前記個々の封止部の不良を検出する工程と、

不良が検出された前記デバイス領域の不良識別表示部にマーキングする工程と、

前記不良識別表示部のマーキングを検出し、不良の前記封止部を取り除く工程とを有することを特徴とする半導体装置の製造方法。

【請求項5】複数のデバイス領域を有し、前記デバイス領域の外部電極形成面に第1～第6の不良識別表示部がそれぞれ形成され、前記複数のデバイス領域のうち、電気的特性の検査により不良が検出されたデバイス領域の前記第1の不良識別表示部にマーキングされた多数個取り基板を準備する工程と、

前記複数のデバイス領域に搭載する半導体チップを準備する工程と、

前記第1の不良識別表示部にマーキングされていない前記デバイス領域に前記半導体チップを搭載する工程と、前記半導体チップの表面電極とこれに対応する前記デバイス領域のボンディング電極とを接続部材によって接続する工程と、

前記半導体チップの表面電極とこれに対応する前記デバイス領域のボンディング電極とが前記接続部材によって接続された前記デバイス領域の不良検査を行う工程と、前記半導体チップのボンディング不良が検出された際には前記デバイス領域の第2の不良識別表示部にマーキングし、前記接続部材の接続不良が検出された際には、前

記デバイス領域の第3の不良識別表示部にマーキングする工程と、

前記多数個取り基板における複数のデバイス領域をモールド樹脂によって一括に覆い、前記半導体チップを樹脂封止するとともに一括封止部を形成する工程と、

前記一括封止部の不良検査を行う工程と、

不良が検出された前記デバイス領域の第4の不良識別表示部にマーキングする工程と、

前記デバイス領域の外部電極形成面に外部電極を形成する工程と、

前記外部電極の不良検出を行う工程と、

不良が検出された前記デバイス領域の第5の不良識別表示部にマーキングする工程と、

ダイシングラインに沿って前記デバイス領域毎に前記多数個取り基板および前記一括封止部を分割して個片化し、個々の封止部を形成する工程と、

前記個々の封止部の不良検出を行う工程と、

不良が検出された前記デバイス領域の第6の不良識別表示部にマーキングする工程と、

20 前記第1～第6の不良識別表示部のマーキングを検出し、不良の前記封止部を取り除く工程とを有することを特徴とする半導体装置の製造方法。

#### 【発明の詳細な説明】

##### 【0001】

【発明の属する技術分野】本発明は、半導体装置の製造技術に関し、特に、一括モールド方式 (MAP : Mold Array Package) により形成された半導体装置の選別に適用して有効な技術に関するものである。

##### 【0002】

【従来の技術】たとえば、CSP (Chip Size Package) などの表面実装形パッケージの半導体装置においては、生産効率を向上して低コスト化を図る技術として、いわゆる一括モールド方式が知られている。

【0003】本発明者が検討したところによれば、一括モールド方式は、複数のデバイス領域が区画されて連なって形成された多数個取りのプリント配線基板を用い、それぞれに半導体チップが搭載された複数のデバイス領域を一括に覆う状態でモールドによって樹脂封止して一括封止部を形成する方法である。

【0004】そして、樹脂封止後、はんだバンプなどの外部端子を形成し、ダイシングを行って多数個取りプリント配線基板および一括封止部をデバイス領域単位に分割(個片化)し、個々のパッケージを形成する。

【0005】また、半導体チップを搭載するプリント配線基板のデバイス領域に配線不良などがある場合には、そのデバイス領域に半導体チップが搭載されることを防止する不良識別の目印が不良個所に設けられている。この不良識別の目印としては、たとえば、不良識別用のシ

50

(4)

5

ール、インキなどによるマーキング、あるいは不良個所表面のけがきなどである。

【0006】その後、個片化された半導体装置は、選別工程において、潜在欠陥の製品などを除去するスクリーニングなどが行われ、良品、不良品の判定が行われる。

【0007】なお、この種の半導体装置について詳しく述べてある例としては、特開平12-12745号公報があり、この文献には、一括モールド方式を用いて組み立てられる半導体装置について記載されている。

[0008]

【発明が解決しようとする課題】ところが、上記のようなMAP方式の半導体装置における製造技術では、次のような問題点があることが本発明者により見い出された。

【0009】すなわち、一括して樹脂封止を行った後に個片化された半導体装置では、不良識別の目印が外観から判別できないために、不良品の管理が困難である。

【0010】そのため、選別工程において、すべての半導体装置の選別検査を行わなければならず、この選別工程のスクリーニングにかかる時間が長くなってしまい、半導体装置の製造効率が低くなってしまうとともに、不良と判別された半導体装置が、どの工程で発生したかなどの分別が難しく、不良解析が困難であるという問題がある。

【0011】本発明の目的は、半導体装置の選別を効率よく、かつ容易に行い、製造コストを小さくすることのできる半導体装置の製造方法を提供することにある。

【0012】本発明の前記ならびにその他の目的と新規な特徴は、本明細書の記述および添付図面から明らかになるであろう。

[0013]

【課題を解決するための手段】本願において開示される発明のうち、代表的なものの概要を簡単に説明すれば、以下のとおりである。

【0014】すなわち、本発明の半導体装置の製造方法は、複数のデバイス領域を有し、該デバイス領域の外部電極形成面に不良識別表示部がそれぞれ形成され、複数のデバイス領域のうち、電気的特性の検査により不良が検出されたデバイス領域の不良識別表示部にマーキングされた多数個取り基板を準備する工程と、複数のデバイス領域に搭載する半導体チップを準備する工程と、不良識別表示部にマーキングされていないデバイス領域に前記半導体チップを搭載する工程と、半導体チップの表面電極とこれに対応するデバイス領域のボンディング電極とを接続部材によって接続する工程と、半導体チップの表面電極とこれに対応するデバイス領域のボンディング電極とが接続部材によって接続されたデバイス領域の不良検査を行う工程と、不良が検出されたデバイス領域の不良識別表示部にマーキングする工程と、多数個取り基板における複数のデバイス領域をモールド樹脂によって

6

一括に覆い、半導体チップを樹脂封止するとともに一括封止部を形成する工程と、ダイシングラインに沿ってデバイス領域毎に多数個取り基板および一括封止部を分割して個片化し、個々の封止部を形成する工程と、不良識別表示部に形成された不良識別マークを検出し、不良の封止部を取り除く工程とを有するものである。

【0015】また、本発明の半導体装置の製造方法は、複数のデバイス領域を有し、該デバイス領域の外部電極形成面に不良識別表示部がそれぞれ形成され、複数のデバイス領域のうち、電気的特性の検査により不良が検出されたデバイス領域の不良識別表示部にマーキングされた多数個取り基板を準備する工程と、複数のデバイス領域に搭載する半導体チップを準備する工程と、不良識別表示部にマーキングされていないデバイス領域に半導体チップを搭載する工程と、半導体チップの表面電極とこれに対応するデバイス領域のボンディング電極とを接続部材によって接続する工程と、半導体チップの表面電極とこれに対応するデバイス領域のボンディング電極とが接続部材によって接続されたデバイス領域の不良検査を行う工程と、不良が検出された前記デバイス領域の不良識別表示部にマーキングする工程と、多数個取り基板における複数のデバイス領域をモールド樹脂によって一括に覆い、半導体チップを樹脂封止するとともに一括封止部を形成する工程と、一括封止部の不良検査を行う工程と、不良が検出された前記デバイス領域の不良識別表示部にマーキングする工程と、ダイシングラインに沿ってデバイス領域毎に多数個取り基板および一括封止部を分割して個片化し、個々の封止部を形成する工程と、不良識別表示部に形成された不良識別マークを検出し、不良の前記封止部を取り除く工程とを有するものである。

【0016】さらに、本発明の半導体装置の製造方法は、複数のデバイス領域を有し、該デバイス領域の外部電極形成面に不良識別表示部がそれぞれ形成され、複数のデバイス領域のうち、電気的特性の検査により不良が検出されたデバイス領域の不良識別表示部にマーキングされた多数個取り基板を準備する工程と、複数のデバイス領域に搭載する半導体チップを準備する工程と、不良識別表示部にマーキングされていないデバイス領域に半導体チップを搭載する工程と、半導体チップの表面電極とこれに対応するデバイス領域のポンディング電極とを接続部材によって接続する工程と、半導体チップの表面電極とこれに対応するデバイス領域のポンディング電極とが接続部材によって接続されたデバイス領域の不良検査を行う工程と、不良が検出されたデバイス領域の不良識別表示部にマーキングする工程と、多数個取り基板における複数のデバイス領域をモールド樹脂によって一括に覆い、半導体チップを樹脂封止するとともに一括封止部を形成する工程と、一括封止部の不良検査を行う工程と、不良が検出された前記デバイス領域の不良識別表示部にマーキングする工程と、デバイス領域の外部電極形

(5)

7

成面に外部電極を形成する工程と、外部電極の不良検出を行う工程と、不良が検出されたデバイス領域の不良識別表示部にマーキングする工程と、ダイシングラインに沿ってデバイス領域毎に多数個取り基板および一括封止部を分割して個片化し、個々の封止部を形成する工程と、不良識別表示部に形成された不良識別マークを検出し、不良の前記封止部を取り除く工程とを有するものである。

【0017】また、本発明の半導体装置の製造方法は、複数のデバイス領域を有し、該デバイス領域の外部電極形成面に不良識別表示部がそれぞれ形成され、複数のデバイス領域のうち、電気的特性の検査により不良が検出されたデバイス領域の不良識別表示部にマーキングされた多数個取り基板を準備する工程と、複数のデバイス領域に搭載する半導体チップを準備する工程と、不良識別表示部にマーキングされていないデバイス領域に半導体チップを搭載する工程と、半導体チップの表面電極とこれに対応するデバイス領域のポンディング電極とを接続部材によって接続する工程と、半導体チップの表面電極とこれに対応するデバイス領域のポンディング電極とが接続部材によって接続されたデバイス領域の不良検査を行う工程と、不良が検出されたデバイス領域の不良識別表示部にマーキングする工程と、多数個取り基板における複数のデバイス領域をモールド樹脂によって一括に覆い、半導体チップを樹脂封止するとともに一括封止部を形成する工程と、該一括封止部の不良検査を行う工程と、不良が検出されたデバイス領域の不良識別表示部にマーキングする工程と、デバイス領域の外部電極形成面に外部電極を形成する工程と、外部電極の不良検出を行う工程と、不良が検出されたデバイス領域の不良識別表示部にマーキングする工程と、ダイシングラインに沿ってデバイス領域毎に多数個取り基板および一括封止部を分割して個片化し、個々の封止部を形成する工程と、個々の封止部の不良を検出する工程と、不良が検出されたデバイス領域の不良識別表示部にマーキングする工程と、不良識別表示部に形成された不良識別マークを検出し、不良の封止部を取り除く工程とを有するものである。

【0018】さらに、本発明の半導体装置の製造方法は、複数のデバイス領域を有し、該デバイス領域の外部電極形成面に第1～第6の不良識別表示部がそれぞれ形成され、複数のデバイス領域のうち、電気的特性の検査により不良が検出されたデバイス領域の第1の不良識別表示部にマーキングされた多数個取り基板を準備する工程と、複数のデバイス領域に搭載する半導体チップを準備する工程と、第1の不良識別表示部にマーキングされていないデバイス領域に半導体チップを搭載する工程と、半導体チップの表面電極とこれに対応するデバイス領域のポンディング電極とを接続部材によって接続する工程と、半導体チップの表面電極とこれに対応するデ

(5)

8

イス領域のポンディング電極とが接続部材によって接続されたデバイス領域の不良検査を行う工程と、半導体チップのポンディング不良が検出された際にはデバイス領域の第2の不良識別表示部にマーキングし、接続部材の接続不良が検出された際には、デバイス領域の第3の不良識別表示部にマーキングする工程と、多数個取り基板における複数のデバイス領域をモールド樹脂によって一括に覆い、半導体チップを樹脂封止するとともに一括封止部を形成する工程と、一括封止部の不良検査を行う工程と、不良が検出されたデバイス領域の第4の不良識別表示部にマーキングする工程と、デバイス領域の外部電極形成面に外部電極を形成する工程と、外部電極の不良検出を行う工程と、不良が検出されたデバイス領域の第5の不良識別表示部にマーキングする工程と、ダイシングラインに沿ってデバイス領域毎に多数個取り基板および一括封止部を分割して個片化し、個々の封止部を形成する工程と、個々の封止部の不良検出を行う工程と、不良が検出されたデバイス領域の第6の不良識別表示部にマーキングする工程と、第1～第6の不良識別表示部に形成された不良識別マークを検出し、不良の封止部を取り除く工程とを有するものである。

【0019】

【発明の実施の形態】以下、本発明の実施の形態を図面に基づいて詳細に説明する。

【0020】図1は、本発明の一実施の形態による半導体装置の断面図、図2は、図1の半導体装置における外観斜視図、図3は、図1の半導体装置の底面図、図4～図10は、図1の半導体装置における製造工程の説明図、図11は、不良の半導体装置に形成された不良識別用パターンの表示例を示した説明図、図12は、図1の半導体装置における製造工程のフローチャートである。

【0021】本実施の形態において、半導体装置1は、表面実装形パッケージの1つであるBGA (Ball Grid Array) からなり、MAP方式によって形成されている。

【0022】この半導体装置1は、図1、および図2に示すように、たとえば、ガラスエポキシ樹脂などからなるプリント配線基板2が設けられている。ここで、プリント配線基板2はプリント基板以外でもよく、たとえば、ポリイミドなどのテープ基板を用いて構成するようにしてよい。

【0023】プリント配線基板2の主面(半導体チップ搭載面)中央部には、絶縁樹脂などの接着材3を介して半導体チップ4が搭載されている。プリント配線基板2の主面において、半導体チップ4の対向する2辺の周辺部近傍には、ポンディング電極2a、ならびに配線パターンが形成されている。

【0024】プリント配線基板2の裏面には、アレイ状に並べられた接続用電極2b(図4)、および配線パターンが形成されている。ポンディング電極2aと接続用

(6)

9

電極 2 b とは、プリント配線基板の両面に形成された配線パターン、ならびにスルーホールなどによって電気的に接続されている。

【0025】また、プリント配線基板 2 裏面の接続用電極 2 b には、球形のはんだからなる複数のはんだバンプ (外部電極) 5 がそれぞれ形成されている。これらはなんだバンプ 5 は、図 3 に示すように、プリント配線基板 2 の裏面上に複数行/複数列 (ここでは、2 行 × 2 列) によって構成されるアレイ状に配列されている。

【0026】さらに、プリント配線基板 2 裏面の中心部近傍には、たとえば、長方形状の不良識別用パターン (不良識別表示部) 6, 7 が形成されている。これら不良識別用パターン 6, 7 は、プリント配線基板 2 に形成された配線パターンに金めっきが施された構成からなる。

【0027】これら不良識別用パターン 6, 7 は、半導体装置 1 の不良を識別する表示用のパターンである。図 3 の左側に位置する不良識別用パターン 6 は、配線不良などを有したプリント配線基板 2 の場合にマーキングされる表示領域であり、右側に位置する不良識別用パターン 7 は、組み立て工程において不良が発生した場合にマーキングされる表示領域である。

【0028】これら不良識別用パターン 6, 7 には、該不良識別用パターン 6, 7 のいずれかにインキなどを塗布することによって不良識別のマーキングを行う。また、不良識別のマーキングは、インキの塗布以外に、不良識別用パターン 6, 7 にカッターなどによってキズをつけたり、あるいは該不良識別用パターン 6, 7 それ自体を除去するようにしてもよい。

【0029】半導体チップ 4 の正面には、図 1、図 2 に示すように、該半導体チップ 4 の外周部近傍に複数の電極 (表面電極) 4 a が形成されている。これら電極 4 a は、ボンディングワイヤ (接続部材) 8 を介して所定のボンディング電極 2 a がそれぞれ接続されている。

【0030】そして、これら半導体チップ 4、プリント配線基板 2 のボンディング電極 2 a 周辺、ならびにボンディングワイヤ 8 が、封止樹脂 9 によって封止されてパッケージ (封止部) が形成されている。

【0031】さらに、半導体装置 1 を電子部品などを実装するプリント実装基板に実装する際には、該プリント実装基板 2 に形成されたランドなどの電極に、はんだバンプ 5 を重合させて搭載し、リフローを行うことにより電気的に接続する。

【0032】次に、本実施の形態における半導体装置 1 の製造工程について、図 1～図 3、および図 4～図 10 の製造工程の説明図、図 11 の不良の半導体装置における不良識別用パターンの説明図、および図 のフローチャートを用いて説明する。

【0033】まず、多数個取り基板 10、および該多数個取り基板 10 に搭載される半導体チップ 4 を準備する

10

(ステップ S101)。この多数個取り基板 10 には、図 4 に示すように、複数のマトリクス配置されたデバイス領域 10 a と、これらデバイス領域 10 a を隔てるダイシングライン 10 b とが形成されており、該複数のデバイス領域 10 a を一括に覆う状態で樹脂モールドされる一括モールドが施される。

【0034】ダイシングライン 10 b は、対になるデバイス領域 10 a 部分、ならびに多数個取り基板 10 とデバイス領域 10 a 部分とを切り離す領域である。デバイス領域 10 a には、前述したボンディング電極 2 a、配線パターン、スルーホール、接続用電極 2 b、および不良識別用パターン 6, 7 などがそれぞれ成形されており、ダイシングして個片化された後、前述したプリント配線基板 2 (図 1) となる。

【0035】また、準備した多数個取り基板 10 において、配線不良などが発生した不良のデバイス領域 10 a のチップ搭載面には、半導体チップ 4 が搭載されることを防止するシールなどの不良識別用の目印が予め形成されており、その反対面 (接続用電極 2 b の形成面) には、不良識別用パターン 6 にインキなどによるマーキングが予め施されている。

【0036】そして、不良識別用パターン 6 にマーキングが施されたデバイス領域 10 a を除くすべてのデバイス領域 10 a の半導体チップ搭載面に接着材 3 をそれぞれ塗布し、図 5 に示すように、半導体チップ 4 を搭載して接着固定する (ステップ S102)。

【0037】その後、図 6 に示すように半導体チップ 4 の電極 4 a と多数個取り基板 10 に形成されたボンディング電極 2 a とをボンディングワイヤ 8 によってそれぞれ接合し、電気的に接続する (ステップ S103)。

【0038】ワイヤボンディングが終了すると、ボンディングワイヤ 8 の接続不良や断線、あるいは半導体チップ 4 の位置ずれなどの組み立て不良を検出する外観検査を行う (ステップ S104)。

【0039】この外観検査において不良が発見された際には (ステップ S105)、図 7 に示すように、デバイス領域 10 a のはんだバンプ形成面に形成されている不良識別用パターン 7 に、インキなどを塗布し、不良識別用のマーキングを行う (ステップ S106)。

【0040】そして、外観検査が終了すると、図 8 に示すように、トランスファーモールド用のモールド金型を用いて一括モールドを行い (ステップ S107)、半導体チップ 4 とボンディングワイヤ 8 とを封止樹脂 9 によって封止し、モールド樹脂を硬化させて一括モールド部 (一括封止部) 11 を形成する。なお、モールド樹脂としては、たとえば、エポキシ系の熱硬化性樹脂などを用いる。

【0041】一括モールド部 11 が形成された後、モールド不良を検査する外観検査を行う (ステップ S108)。この外観検査において不良が発見された際には

(7)

11

(ステップS109)、ステップS106の処理と同様に、該当する不良のデバイス領域10aに形成されている不良識別用パターン7にインキなどを塗布し、不良識別のマーキングを行う(ステップS110)。

【0042】その後、図9に示すように、多数個取り基板10の裏面に形成されている接続用電極2b(図4)に、はんだバンプ5をそれぞれ形成する(ステップS111)。

【0043】はんだバンプ5は、たとえば、多数個取り基板10の半導体チップ4搭載面を下方に向け、複数のはんだバンプ5を真空吸着保持したボール搭載用治具をその上方に配置し、多数個取り基板10の上方から各デバイス領域10a上の接続用電極に搭載して形成する。

【0044】これらははんだバンプ5の形成後、該はんだバンプ5の形成に不良がないかを外観検査する(ステップS112)。この外観検査で不良が発見された際には(ステップS113)、ステップS106、S110の処理と同様に、該当する不良のデバイス領域10aに形成されている不良識別用パターン7にインキなどを塗布し、不良識別のマーキングを行う(ステップS114)。

【0045】そして、多数個取り基板10のダイシングライン10bに沿って、個々のデバイス領域10aを個片化する。この場合、図10に示すように、ダイシング用の切断刃であるブレードBを用いたダイシングによって該一括モールド部11を分割して個片化し(ステップS115)、個々のパッケージが形成される。

【0046】その後、個片化されたパッケージの外観検査を行い(ステップS116)、この外観検査で不良が発見された際には(ステップS117)、ステップS106、S110、S114の処理と同様に、該当する不良のデバイス領域10aに形成されている不良識別用パターン7にインキなどを塗布し、不良識別のマーキングを行う(ステップS118)。

【0047】個片化された後、半導体装置1は、良品と不良品とに選別され(ステップS119)、半導体装置1が完成する(ステップS120)。

【0048】ここで、不良の半導体装置1には、図11に示すように、プリント配線基板2に形成された不良識別用パターン6、7のいずれかにインキによるマーキングが施されているので、選別の際には、半導体装置1に形成された不良識別用パターン6、7のいずれかのマーキングを確認することにより、該半導体装置1を選別する。

【0049】それにより、本実施の形態によれば、多数個取り基板10の不良、および組み立て不良となった半導体装置だけを短時間で効率よく取り除くことができ、半導体装置1の製造コストを小さくすることができる。

【0050】また、多数個取り基板10による不良と、組み立て工程などによる不良とを簡単に判別するこ

12

できるので、不良となった半導体装置の不良解析を容易にすることができます。

【0051】また、本実施の形態では、多数個取り基板10の不良と組み立て工程の不良とを示す2つの不良識別用パターン6、7をプリント配線基板2の接続用電極2b形成面側に設けた構成としたが、図13、図14に示すように、半導体装置1aに6つの不良識別用パターン12～17を設け、不良工程をより詳細に判別できるようにしてもよい。

【0052】不良識別用パターン(第1の不良識別表示部)12は、配線不良などの基板不良の際にマーキングされるパターンである。不良識別用パターン(第2の不良識別表示部)13は、チップ位置ずれなどのチップポンディング時の不良の際にマーキングされ、不良識別用パターン(第3の不良識別表示部)14は、ポンディングワイヤの接続不良などのワイヤポンディングの不良の際にマーキングされる。

【0053】さらに、不良識別用パターン(第4の不良識別表示部)15は、一括モールド部の形成不良の際にマーキングされるパターンである。不良識別用パターン(第5の不良識別表示部)16は、はんだバンプ5の形成不良の際にマーキングされる。

【0054】不良識別用パターン(第6の不良識別表示部)17は、ダイシング時のパッケージ形成不良が発生した際にマーキングされるパターンである。そして、これら不良識別用パターン12～17は、カッターなどによってキズをつけるか、あるいはインキなどを塗布することによってマーキングされる。

【0055】それにより、組み立て工程の不良を、より詳しく表示することができるので、不良の半導体装置を短時間で効率よく取り除くことができるとともに、不良解析をより容易に行うことができる。

【0056】以上、本発明者によってなされた発明を発明の実施の形態に基づき具体的に説明したが、本発明は前記実施の形態に限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない。

【0057】たとえば、前記実施の形態では、半導体装置における接続用電極形成面側の中央部近傍に不良識別用パターンを設けた構成としたが、半導体装置1に形成されるこれら不良識別用パターン6、7は、図15に示すように、プリント配線基板2の外周部近傍など、該接続用電極2bに接触しなければ、形成される位置や形状などは問わない。

【0058】

【発明の効果】本願によって開示される発明のうち、代表的なものによって得られる効果を簡単に説明すれば、以下のとおりである。

【0059】(1) 多数個取り基板の不良、ならびに組み立て不良の半導体装置だけを短時間で効率よく取り除

(8)

13

くことができるので、半導体装置の製造コストを小さくすることができる。

【0060】(2) 多数個取り基板の不良と組み立て工程での不良とを簡単に判別することができる。不良となった半導体装置の不良解析を容易に、かつ効率よく行うことができる。

【図面の簡単な説明】

【図1】本発明の一実施の形態による半導体装置の断面図である。

【図2】図1の半導体装置における外観斜視図である。

【図3】図1の半導体装置の底面図である。

【図4】図1の半導体装置における製造工程の説明図である。

【図5】図4に続く半導体装置の製造工程の説明図である。

【図6】図5に続く半導体装置の製造工程の説明図である。

【図7】図6に続く半導体装置の製造工程の説明図である。

【図8】図7に続く半導体装置の製造工程の説明図である。

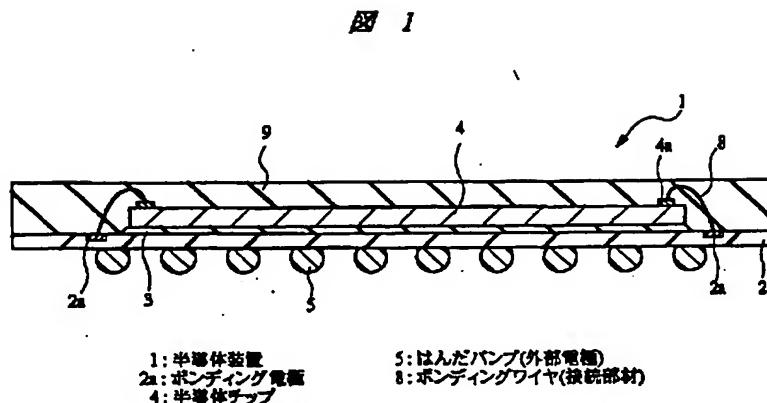
【図9】図8に続く半導体装置の製造工程の説明図である。

【図10】図9に続く半導体装置の製造工程の説明図である。

【図11】不良の半導体装置に形成された不良識別用パターンの表示例を示した説明図である。

【図12】図1の半導体装置における製造工程のフローチャートである。

【図1】



14

【図13】本発明の他の実施の形態による不良識別用パターンが設けられた半導体装置の底面図である。

【図14】図13の半導体装置における不良識別用パターンの拡大説明図である。

【図15】本発明の他の実施の形態による不良識別用パターンが設けられた半導体装置の底面図である。

【符号の説明】

- 1 半導体装置
- 1 a 半導体装置
- 2 プリント配線基板
- 2 a ボンディング電極
- 2 b 接続用電極
- 3 粘着材
- 4 半導体チップ
- 4 a 電極(表面電極)
- 5 はんだバンプ(外部電極)
- 6, 7 不良識別用パターン(不良識別表示部)
- 8 ボンディングワイヤ(接続部材)
- 9 封止樹脂
- 10 多数個取り基板
- 10 a デバイス領域
- 10 b ダイシングライン
- 11 一括モールド部(一括封止部)
- 12 不良識別用パターン(第1の不良識別表示部)
- 13 不良識別用パターン(第2の不良識別表示部)
- 14 不良識別用パターン(第3の不良識別表示部)
- 15 不良識別用パターン(第4の不良識別表示部)
- 16 不良識別用パターン(第5の不良識別表示部)
- 17 不良識別用パターン(第6の不良識別表示部)

【図2】

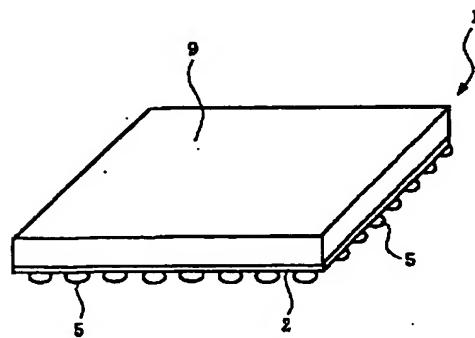
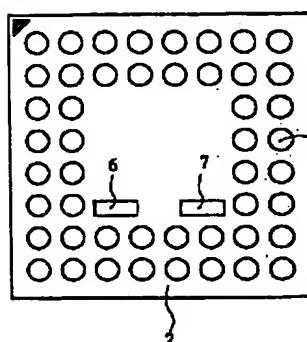


図2

(9)

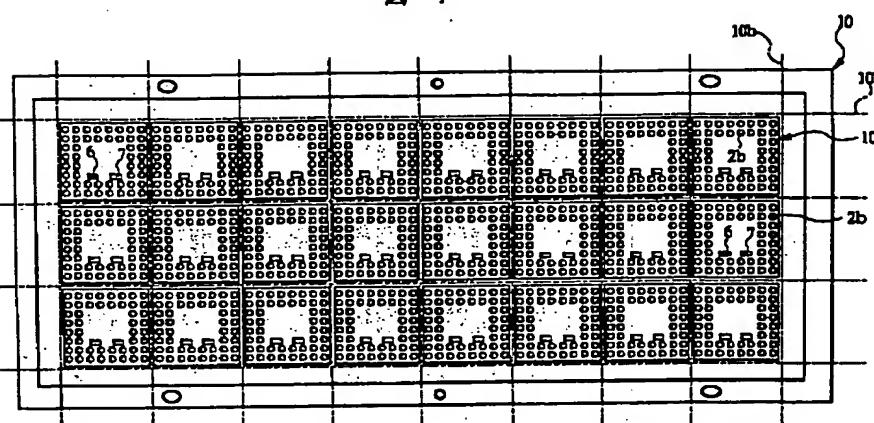
【図3】

図3



【図4】

図4



2b: 接続用電極  
6: 不良識別用パターン(不良識別表示部)  
7: 不良識別用パターン(不良識別表示部)

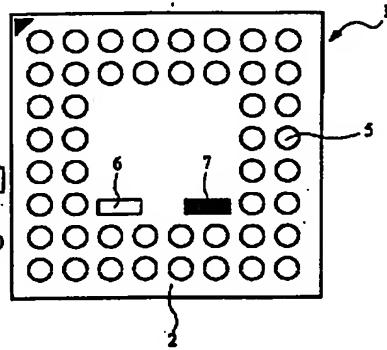
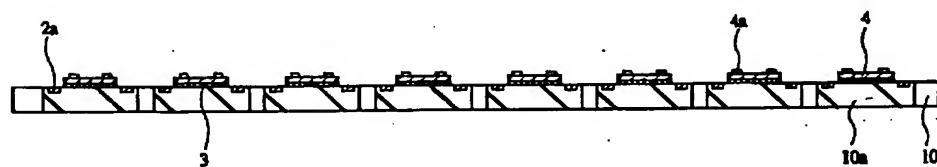
10: 多数端取り基板  
10a: デバイス領域  
10b: ダイシングライン

11: 一括モールド部(一括封止部)

【図5】

【図11】

図5

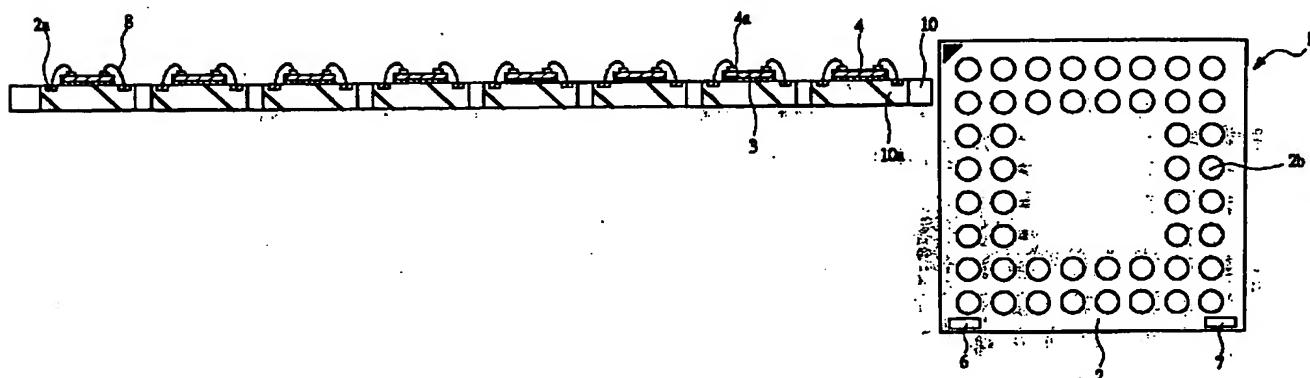


【図6】

図6

【図15】

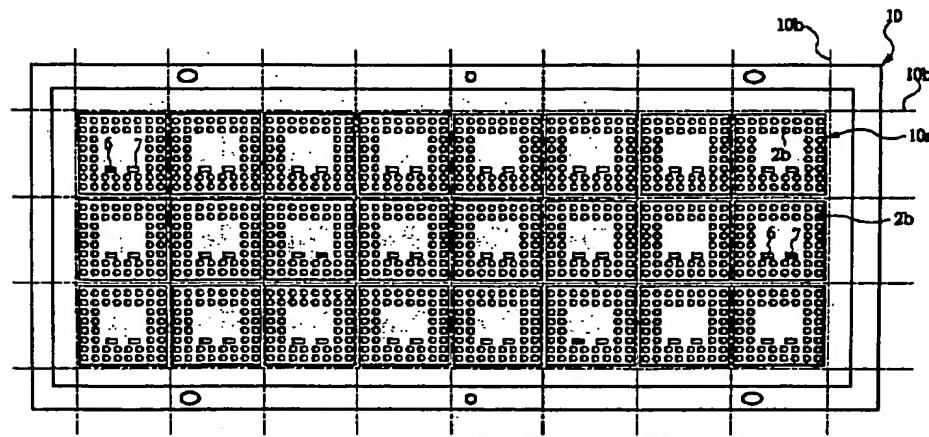
図15



(10)

【図7】

図7



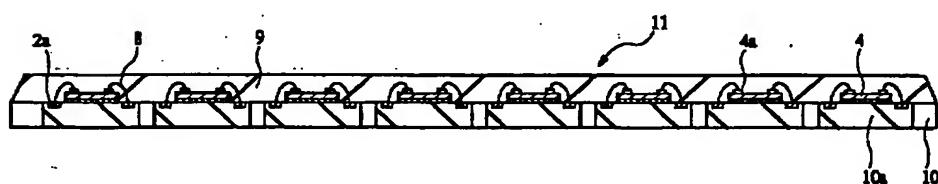
2b:接続用電極  
6:不良識別用パターン(不良識別表示部)  
7:不良識別用パターン(不良識別表示部)

10:多段取り基板  
10a:デバイス領域  
10b:ダイシングライン

11:一括モールド部(一括封止部)

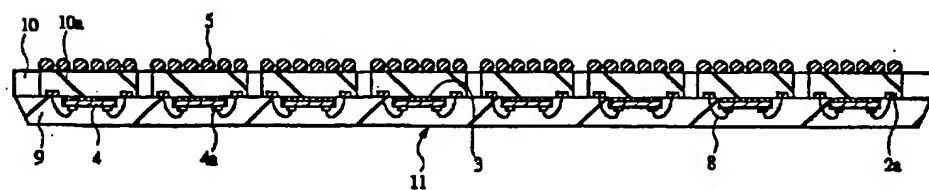
【図8】

図8



【図9】

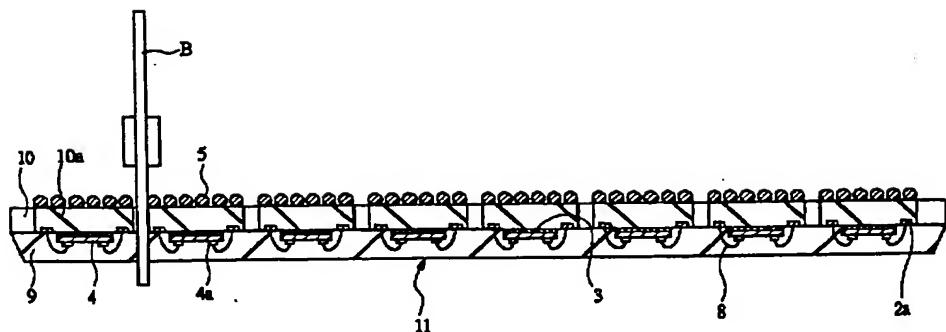
図9



(11)

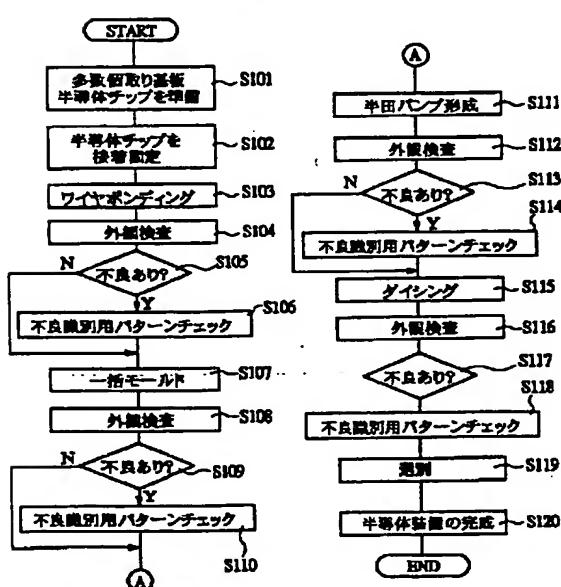
[図10]

10



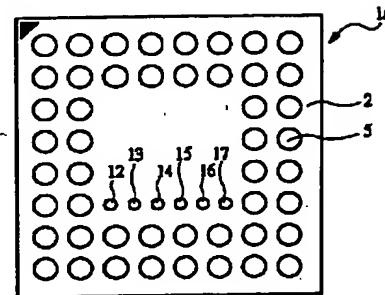
【图12】

图 12



[図13]

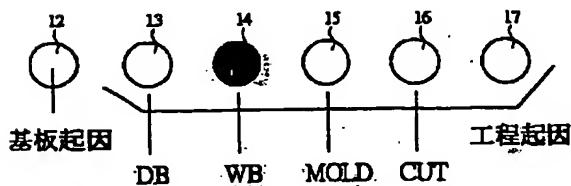
87 13



- 1a: 半導体監視
- 12: 不良識別用パターーン第1の不良識別表示部
- 13: 不良識別用パターーン第2の不良識別表示部
- 14: 不良識別用パターーン第3の不良識別表示部
- 15: 不良識別用パターーン第4の不良識別表示部
- 16: 不良識別用パターーン第5の不良識別表示部
- 17: 不良識別用パターーン第6の不良識別表示部

[図14]

14



(12)

フロントページの続き

(72)発明者 黒田 宏  
東京都小平市上水本町五丁目20番1号 株  
式会社日立製作所半導体グループ内

F ターム(参考) 5F061 AA01 BA03 CA21 CB12 CB13  
GA01

**This Page is Inserted by IFW Indexing and Scanning  
Operations and is not part of the Official Record**

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- BLACK BORDERS**
- IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- FADED TEXT OR DRAWING**
- BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- SKEWED/SLANTED IMAGES**
- COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- GRAY SCALE DOCUMENTS**
- LINES OR MARKS ON ORIGINAL DOCUMENT**
- REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- OTHER:** \_\_\_\_\_

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.**